Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method of manufacturing an integrated circuit having a gate structure above a substrate including germanium, the method comprising:

forming a first layer above the gate structure and above the substrate;

forming a second layer above the first layer; and

doping source and drain regions through the first layer and the second layer, whereby germanium back sputtering is reduced.

2. (Original) The method of claim 1, further comprising:

annealing the substrate whereby the first layer and the second layer prevent outgassing.

3. (Original) The method of claim 1, wherein the first layer includes at least one of silicon dioxide and silicon carbide.

4. (Original) The method of claim 1, wherein second layer includes at least one of silicon nitride, titanium, titanium nitride, titanium/titanium nitride, tantalum nitride, and silicon carbide.

5. (Original) The method of claim 1, wherein the steps of forming a first layer and forming a second layer utilize low temperature deposition.

6. (Original) The method of claim 5, wherein the low temperature deposition is performed at a temperature below approximately 800°C.

7. (Original) The method of claim 5, wherein the low temperature deposition is a chemical vapor deposition process.

8. (Original) The method of claim 1, further comprising:

providing a rapid thermal anneal.

9. (Original) A method of forming source and drain regions in a strained semiconductor layer, the method comprising:

providing a first layer comprising at least one of silicon nitride and silicon dioxide above the strained semiconductor layer;

providing a second layer above the first layer, the second layer containing nitrogen, titanium, tantalum, or carbon;

implanting non-neutral dopants into the strained semiconductor layer; and

annealing the strained semiconductor layer.

10. (Original) The method of claim 9, wherein the annealing step is a rapid thermal anneal for activating the dopants.

11. (Original) The method of claim 10, further comprising:

removing the second layer after the annealing step.

12. (Original) The method of claim 9, further comprising:

providing an insulative material above the first layer.

13. (Original) The method of claim 12, wherein the first layer includes silicon dioxide and the insulative material includes silicon nitride.

14. (Original) The method of claim 9, wherein the anneal is a rapid thermal anneal at a temperature above 600°C.

15. (Original) The method of claim 14, wherein the first layer is deposited in a low temperature process.

16. (Original) The method of claim 15, wherein the layer containing titanium, nitrogen, tantalum or carbon is provided in a low temperature process.

17. (Currently Amended) A method of fabricating a transistor in a germanium containing layer, the method comprising:

providing a gate structure above the germanium containing layer;

providing a first layer of insulative material in a low temperature process above the germanium containing layer;

doping the germanium containing layer through the first layer to form source and drain regions; and

annealing the germanium containing layer to activate dopants in the source and drain regions.

18. (Original) The method of claim 17, wherein the step of providing a first layer is an LPCVD deposition process performed at a low temperature.

19. (Original) The method of claim 18, wherein the step of providing a first layer utilizes an oxygen atmosphere and silane atmosphere.

20. (Original) The method of claim 19, further comprising:

depositing a second layer over the first layer before the doping step.